

## CLAIMS

1. A phase-locked loop circuit for demodulating a Radio Data System (RDS) signal superimposed on an ARI signal component of a stereo-multiplex signal, the circuit comprising:

an oscillator that generates an in-phase component signal and a quadrature component signal of the carrier of the RDS signal;

a first circuit branch comprising a first multiplier having a first input at which a sampled stereo-multiplex signal is received and a second input at which the in-phase component signal is received, a first low-pass filter having an input connected to an output of the first multiplier, a first divider having an input connected to an output of the first low-pass filter, and a first high-pass filter having an input connected to an output of the first divider;

a second circuit branch comprising a second multiplier having a first input at which the sampled stereo-multiplex signal is received, and a second input at which the quadrature component signal is received, a second low-pass filter having an input connected to an output of the second multiplier, a second divider having an input connected to an output of the second low-pass filter, and a second high-pass filter having an input connected to an output of the second divider;

a feedback branch comprising an arithmetic unit having first and second inputs connected to outputs of the first and second high-pass filters, respectively, a clock input at which an RDS bit clock signal is received, and an output at which the arithmetic unit generates an error signal; a filter having an input at which it receives the error signal, and an output at which it generates a filtered error signal; a control unit having an input connected to the filter output, and an output connected to a control input of the oscillator at which the control unit generates a control signal in response to the error signal;

a clock generator having a first control input connected to the output of the first high-pass

23 filter, a second control input connected to an output of the oscillator, and an output at which the  
24 clock generator generates the RDS bit clock signal; and  
25 an RDS decoder having a first input connected to the output of the first high-pass filter, a  
26 clock input at which the RDS bit clock signal is received, and an output from which RDS data is  
27 retrievable.

1 2. The phase-locked loop circuit according to Claim 1, wherein the filter comprises a loop filter.

1 3. The phase-locked loop circuit according to Claim 1, wherein the sampling frequency for the  
2 stereo-multiplex signal is selected such that the spectrum of the RDS signal in the region around the  
3 carrier of the RDS signal is represented completely by the sampled stereo-multiplex signal.

1 4. The phase-locked loop circuit according to Claim 1, wherein the sampling frequency is  
2 selected to be greater than 120 kHz.

1 5. The phase-locked loop circuit according to Claim 1, wherein the first and second dividers  
2 divide the low-pass filtered signals presented at their respective inputs by a division factor of 16.

1 6. The phase-locked loop circuit according to Claim 1, wherein the oscillator comprises a  
2 digital oscillator.

1 7. The phase-locked loop circuit according to Claim 1, wherein the arithmetic unit calculates the  
2 error signal at those times when the amplitude of the in-phase component is at maximum.

1 8. The phase-locked loop circuit according to Claim 1, wherein the oscillator is synchronized  
2 with the carrier of the RDS signal, wherein prior to synchronization, the arithmetic unit shifts the  
3 calculation cycle for the error signal by a quarter-bit clock period upon detection of a zero crossing of  
4 the amplitude of the in-phase component.

1 9. A method for demodulating a Radio Data System (RDS) signal superimposed on an ARI  
2 signal component of a stereo-multiplex signal, the method comprising:

3 generating an in-phase component signal and a quadrature component signal of the carrier of  
4 the RDS signal;

5 multiplying a sampled stereo-multiplex signal by the in-phase component to generate a first  
6 product signal;

7 low-pass filtering the first product signal to generate a first low-pass filtered signal;

8 dividing a sampling rate of the first low-pass-filtered signal by a first presettable division  
9 factor to generate a decimated, filtered first product signal;

10 high-pass filtering the decimated, filtered first product signal to generate a first high-pass-  
11 filtered signal;

12 decoding the first high-pass filtered signal to generate RDS data;

13 multiplying the sampled stereo-multiplex signal by the quadrature component of the digital  
14 oscillator to generate a second product signal;

15 low-pass filtering the second product signal to generate a second low-pass filtered signal;

16 dividing a sampling rate of the second low-pass-filtered signal by a second presettable  
17 division factor to generate a decimated, filtered second product signal;

18 high-pass filtering the decimated, filtered second product signal to generate a second high-

19 pass-filtered signal;  
20 calculating an error signal representing a phase difference between the carrier of the RDS  
21 signal and the output signal of the oscillator based on the first and second high-pass-filtered signals  
22 and an RDS clock signal, wherein the error signal represents a phase position between the carrier of  
23 the RDS signal and the output signal of the oscillator; and  
24 generating a correction signal for controlling the oscillator based on the error signal.

1 10. The method for demodulating a RDS signal according to Claim 9, further comprising the step  
2 of:

3 filtering the error signal prior to using the error signal to generate the correction signal.

1 11. The method for demodulating a RDS signal according to Claim 10, wherein the step of  
2 filtering the error signal comprises the step of:

3 filtering the error signal with a loop filter.

1 12. The method according to Claim 9, further comprising the steps of:

2 selecting, prior to the step of generating in-phase and quadrature component signals, a  
3 sampling frequency for the stereo-multiplex signal such that the spectrum of the RDS signal in the  
4 region around the carrier of the RDS signal is represented completely by the digital signal.

1 13. The method according to Claim 12, wherein the sampling frequency is selected to be greater  
2 than 120 kHz.

1 14. The method according to Claim 9, wherein the first presettable division factor is 16.

1 15. The method according to Claim 9, wherein the second presettable division factor is 16.

1 16. The method according to Claim 9, wherein the oscillator includes a digital oscillator.

1 17. The method according to Claim 9, wherein the RDS bit clock signal is generated by a clock  
2 generator in response to the oscillator and the first high-pass-filtered signal.

1 18. The method according to Claim 17, wherein the step of decoding the first high-pass filtered  
2 signal to generate RDS data is performed by an RDS decoder that is clocked by the RDS bit clock  
3 signal.

1 19. The method according to Claim 1, wherein the step of calculating the error signal is  
2 performed at those times when the amplitude of the in-phase component is at maximum.

1 20. The method according to Claim 1, wherein the oscillator is synchronized with the carrier of  
2 the RDS signal, and wherein the step of calculating the error signal comprises the step of:  
3 shifting the calculation cycle for the error signal by a quarter-bit clock period upon detection  
4 of a zero crossing of the amplitude of the in-phase component.

1 21. The method according to Claim 1 wherein the method is implemented as a software program  
2 stored in a computer-readable medium.

1 22. A phase-locked loop circuit for demodulating a Radio Data System (RDS) signal  
2 superimposed on an ARI signal component of a stereo-multiplex signal, the circuit comprising:  
3 oscillator means for generating an in-phase component signal and a quadrature component  
4 signal of an RDS carrier signal in response to an oscillator control signal;  
5 means for generating a first product signal of a sampled stereo-multiplex signal and the in-  
6 phase component signal;

means for generating a second product signal of a sampled stereo-multiplex signal and the quadrature component signal;

means for controlling the oscillator based on the phase relationship between the RDS carrier signal and the signals generated by the oscillator; and

means for generating RDS data based on the first high-pass filter.

23. The phase-locked loop circuit according to Claim 22, wherein the means for generating a first product signal comprises:

means for multiplying a sampled stereo-multiplex signal by the in-phase component to generate a first product signal;

means for low-pass filtering the first product signal to generate a first low-pass filtered signal;

means for low-pass filtering the first product signal to generate a first low-pass filtered signal;

and

means for high-pass filtering the decimated, filtered first product signal to generate a first high-pass-filtered signal.

24. The phase-locked loop circuit according to Claim 22, wherein the means for generating a second product signal comprises:

means for multiplying the sampled stereo-multiplex signal by the quadrature component of the digital oscillator to generate a second product signal;

means for low-pass filtering the second product signal to generate a second low-pass filtered signal;

means for dividing a sampling rate of the second low-pass-filtered signal by a second presettable division factor to generate a decimated, filtered second product signal; and

9 means for high-pass filtering the decimated, filtered second product signal to generate a  
10 second high-pass-filtered signal.

1 25. The phase-locked loop circuit according to Claim 22, wherein the means for controlling the  
2 oscillator comprises:

3 means for calculating an error signal representing a phase difference between the RDS carrier  
4 signal and the oscillator based on the first and second product signals, wherein the error signal  
5 represents a phase position between the RDS carrier signal and the output signal of the oscillator;  
6 and

7 means for generating the oscillator control signal based on the error signal.

1 26. The phase-locked loop circuit according to Claim 22, wherein the sampling frequency for the  
2 stereo-multiplex signal is selected such that the spectrum of the RDS signal in the region around the  
3 carrier of the RDS signal is represented completely by the sampled stereo-multiplex signal.

1 27. The phase-locked loop circuit according to Claim 22, wherein the first and second divider  
2 means divide the received low-pass filtered signals by a division factor of 16.

1 28. The phase-locked loop circuit according to Claim 22, wherein the arithmetic unit calculates  
2 the error signal is calculated at those times when the amplitude of the in-phase component is at  
3 maximum.

1 29. The phase-locked loop circuit according to Claim 25, wherein the oscillator means is  
2 synchronized with the carrier of the RDS signal, wherein prior to synchronization, wherein the  
3 means for generating an error signal shifts the calculation cycle for the error signal by a quarter-bit

- 4 clock period upon detection of a zero crossing of the amplitude of the in-phase component.